REMARKS

Claim Objections

The Examiner has objected to claim 5 because claim 5 depends from claim 14. The Examiner stated that this does not appear to make sense, and it appears that claim 5 should depend from claim 4.

Claim 5 has been amended to be dependent on claim 1.

35 U.S.C. § 112 Rejections

The Examiner has rejected claims 1, 3, and 5-20 under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The Examiner has rejected claims 1, 3, and 5-20, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The Examiner has rejected claims 1, 3, and 5-20, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Examiner stated that the specification alleges that the present invention can be practiced with only some of the aspects or without the specific details, that the order of the invention is irrelevant, and that repeated usage of the phrase "in one

embodiment" does not necessarily refer to the same embodiment, although it may. The Examiner also stated that such statements in the specification are confusing and an attempt to add material which had not been expressly disclosed or properly incorporated. The Examiner further stated that the specification contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention without undo experiment.

Applicant respectfully submits that the statements to which the Examiner refers are commonly found in modern patent applications in anticipation of the particular patent application going to litigation. As the Examiner will appreciate, a common tactic used in litigating a particular patent application is to attempt to limit the allowed claims in such a way that they are interpreted to cover only the embodiments specifically disclosed in the detailed description. The statements listed above simply reiterate the fact that the present invention is not meant to be limited to the specific embodiments described in the specification. Applicant respectfully submits that one skilled in the art would appreciate that not all of the specific details described in the specification are necessary to practice the present invention, that the operations described in the specification do not necessarily need to be performed in the order they are presented, and that the phrase "in one embodiment" does not necessarily refer to the exact same embodiment.

35 U.S.C. § 103 Rejections

The Examiner has rejected claims 1, 3, 5, and 8-20 under 35 U.S.C. § 103(a) as being unpatentable over Bhatia or Lin in view of Hafizi, or Herbert, or Rankin.

Claims 1, 11, 15, and 19 include determining a maximum data rate based on characteristics of the integrated circuit and adjusting the operation of the integrated circuit to not exceed the maximum data rate. Specifically, claims 1, 11, 15, and19 include the limitations "determining a sustainable power level for an integrated circuit based upon environmental system thermal characteristics and design characteristics," "translating the sustainable power level into a data transfer rate," and "adjusting operation of the integrated circuit such that the data transfer rate is not exceeded."

Bhatia does not teach or suggest determining a maximum data rate based on characteristics of the integrated circuit and adjusting the operation of the integrated circuit to not exceed the maximum data rate. Bhatia teaches a system including a processor with a clock and a thermal management controller that monitors a temperature in the system and varies the component between different performance states when an over-temperature condition is detected (Abstract). Referring to Figure 1, an example system 10 includes processors 12 and temperature sensor units 15 that monitor system temperature in one or more corresponding thermal zones (col. 3, lines 25-35). When the monitored temperature is above a particular temperature a thermal engage SMI is generated, and when the monitor temperature is below the particular temperature, a thermal disengage SMI is generated. The SMI may be generated at periodic intervals to allow software or firmware to manage the performance level of the

processor (col. 3, lines 48-55). Bhatia thus teaches altering the performance of an integrated circuit based on sensed temperatures within different zones around the integrated circuit. Bhatia does not teach or suggest determining a maximum data rate based on characteristics of the integrated circuit and adjusting the operation of the integrated circuit to not exceed the maximum data rate.

Lin does not teach or suggest determining a maximum data rate based on characteristics of the integrated circuit and adjusting the operation of the integrated circuit to not exceed the maximum data rate. Lin teaches an over-temperature protection method and its device for a central processing unit (Abstract). Figure 1 shows a flow chart of the over-temperature protection method for a CPU of the present invention, and on/off instruction, and an instruction for identifying the type of CPU are pre-stored in a read and write memory unit (BIOS) so that when operation of the computer is initiated 20, CPU 30 will directly read the above-mentioned instruction from the BIOS memory unit 10 and instruct a chip circuit 40 to operate, and at the same time energize on/off function circuit 50 (col. 2, lines 22-31). As the working temperature of the CPU 30 rises, the value of temperature sensing heat sensitive resistance 70 decreases linearly, and the potential of the resistor connected to its one terminal will increase inversely proportional to a starting value as soon as the working temperature of the CPU 30 reaches a predetermined value (col. 2, lines 39-44). Lin thus discloses an over-temperature protection method for a central processing unit based on the temperature of various components within the unit. Specifically, Lin does not teach or suggest determining a maximum data rate based on characteristics of the integrated

circuit and adjusting the operation of the integrated circuit to not exceed the maximum data rate.

Hafizi does not teach or suggest determining a maximum data rate based on characteristics of the integrated circuit and adjusting the operation of the integrated circuit to not exceed the maximum data rate. Hafizi teaches the reliability of high-performance AlInAs/GaInAs heterojunction bipolar transistors. Devices with a base Be doping level of $5x10^{19}$ cm^{-3} and a base thickness of approximately 50 nm displayed no sign of Be diffusion under applied bias. Excellent stability in DC current gain, device turn-on voltage, and base-emitter junction characteristics was observed. Accelerated life-test experiments were performed under an applied constant collector current density of $7x10^4$ A/cm^2 at ambient temperatures of 193, 208, and 328°C. Junction temperature and device thermal resistance were determined experimentally. Degradation of the base-collector junction was used as failure criterion to project a mean time to failure in excess of 10^7 h at 125°C junction temperature with an associated activation energy of 1.92 eV. Hafizi does not teach or suggest determining a maximum data rate based on characteristics of the integrated circuit and adjusting the operation of the integrated circuit to not exceed the maximum data rate.

Herbert does not teach or suggest determining a maximum data rate based on characteristics of the integrated circuit and adjusting the operation of the integrated circuit to not exceed the maximum data rate. Herbert teaches a clock rate for a device that is controlled through the use of integrated circuits which respond to the temperature of the device (Abstract). Figure 1 depicts a diode-based temperature

sensing circuit 10. When the current through diode D1 exceeds some threshold value at 16, as determined by the resistor divider network R2 and R3 output 18 of the comparator (differential amplifier 12) goes HIGH indicating that the threshold temperature has been reached (col. 3, lines 61-66). The output 18 of comparator 12 is used in the preferred embodiment as a control signal to select various clock rates (col. 3, line 66 - col. 4, line 1). Herbert thus teaches regulating the clock rates for integrated circuits based on temperatures within the device. Specifically, Herbert does not teach or suggest determining a maximum data rate based on characteristics of the integrated circuit and adjusting the operation of the integrated circuit to not exceed the maximum data rate.

Rankin does not teach or suggest determining a maximum data rate based on characteristics of the integrated circuit and adjusting the operation of the integrated circuit to not exceed the maximum data rate. Rankin teaches a method and apparatus for power throttling to manage the temperature of an integrated circuit (Abstract). A junction temperature for the integrated circuit is determined and compared to a thermal maximum value that is less than a predetermined value for the integrated circuit. Power consumption of the integrated circuit is reduced when the junction temperature reaches a predetermined value (col. 1, lines 37-42). Rankin thus teaches regulating the power to an integrated circuit based on the temperature of the integrated circuit. Specifically, Rankin does not teach or suggest determining a maximum data rate based on characteristics of the integrated circuit and adjusting the operation of the integrated circuit to not exceed the maximum data rate.

Therefore, claims 1, 11, 15, and 19 are patentable over Bhatia or Lin in view of Hafizi, or Herbert, or Rankin because claims 1, 11, 15, and 19 include limitations that are not taught or suggested by Bhatia, Lin, Hafizi, Herbert, and Rankin.

Claims 3, 5, 9, 10, 12-14, 16-18, and 20 are dependent on either claim 1, claim 11, claim 15, or claim 19 and should be allowable for the same reasons as claims 1, 11, 15, and 19 stated above.

Claim 8 has been cancelled.

Applicant, accordingly, respectfully requests withdrawal of the rejections of claims 1, 3, 5, and 9-20 under 35 U.S.C. § 103(a) as being unpatentable over Bhatia or Lin in view of Hafizi, or Herbert, or Rankin.

The Examiner has rejected claims 6 and 7 under 35 U.S.C. § 103(a) as being unpatentable over Bhatia or Lin in view of Hafizi, or Herbert, or Rankin, and further in view of Woo or Bogin.

Claims 6 and 7 are dependent on claim 1 and should be allowable for the same reasons as claim 1 stated above.

Applicant, accordingly, respectfully requests withdrawal of the rejections of claims 6 and 7 under 35 U.S.C. § 103(a) as being unpatentable over Bhatia or Lin in view of Hafizi, or Herbert, or Rankin and further in view of Woo or Bogin.

Applicant respectfully submits that the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call John P. Ward at (408) 720-8300.

Pursuant to 37 C.F.R. 1.136(a)(3), applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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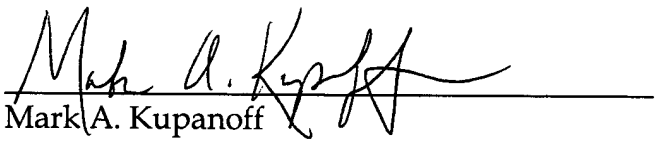

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